We Claim:

1. A method for generating a clock pulse in a data processing system having a plurality of independent, non-synchronous digital data channels, which comprises the steps of:

deriving a reference clock pulse;

supplying the reference clock pulse to the data channels; and

compensating for differences in a clock pulse frequency between the reference clock pulse and each of the data channels using a delay-locked loop circuit.

2. The method according to claim 1, which comprises deriving the reference clock pulse using a phase-locked loop circuit and data provided by one of the data channels serving as a reference channel.

3. The method according to claim 1, which comprises deriving the reference clock pulse from an independent clock generator.

4. The method according to claim 1, which comprises continuously adapting a phase of the reference clock pulse, for each of the data channels, to a phase of the each of the data channels using the delay-locked loop circuit associated

with each of the data channels resulting in an adapted reference clock pulse for each of the data channels.

5. The method according to claim 4, which comprises sampling data from each of the data channels using the adapted reference clock pulse.

6. The method according to claim 1, which comprises deriving the reference clock pulse from a quartz oscillator.

7. The method according to claim 1, which comprises deriving the reference clock pulse using a phase-locked loop circuit and a co-supplied clock pulse from one of the data channels serving as a reference channel.

8. A configuration for generating a clock pulse in a data processing system having a plurality of independent, non-synchronous digital data channels, the configuration comprising:

a device for generating a reference clock pulse; and

a plurality of signal sensor blocks each allocated to one of the data channels and each connected to said device for receiving the reference clock pulse, each of said signal sensor blocks having a delay-locked loop circuit for

compensating for differences in a clock frequency between the reference clock pulse and a respective data channel, said delay-locked loop circuit having an infinite delay range and a bandwidth larger than the difference between the clock frequency of the reference clock pulse and the clock frequency of the respective data channel.

9. The configuration according to claim 8, wherein said device for generating the reference clock pulse includes a phase-locked loop circuit for deriving the reference clock pulse from one of data and a co-supplied clock pulse from one of the data channels serving as a reference channel.

10. The configuration according to claim 8, wherein said device for generating the reference clock pulse includes a clock generator.

11. The configuration according to claim 8, wherein said delay-locked loop circuit has a phase detector, a charge pump connected to the phase detector, and a phase modifier connected to said charge pump.

12. The configuration according to claim 8, wherein each of the data channels are identically constructed and each of said signal sensor blocks are identically constructed.

13. The configuration according to claim 8, including a receiver module to be connected to the data channels.

14. The configuration according to claim 13, wherein said receiver module is a demultiplexer.

15. The configuration according to claim 8, wherein said device for generating the reference clock pulse includes a quartz oscillator.

16. The configuration according to claim 8, including a transmitter module to be connected to the data channels.

17. The configuration according to claim 16, wherein said transmitter module is a multiplexer.